REMARKS

Claims 1-28 are all the claims pending in the application. Claims 8-15 and 22-26 were withdrawn from further consideration by virtue of the Response to Restriction Requirement filed February 3, 2006. No new matter is presented.

As an initial matter, Applicant notes that the Examiner has not considered the non-patent literature documents submitted in the Information Disclosure Statement of September 22, 2003. Applicant further notes that these documents are discussed in the at paragraph 6 of the specification, and the IDS clearly indicates that the concise statement of relevance is provided by the discussion of the documents in the specification. Thus, the Examiner's refusal to consider these documents is improper. Applicant therefore kindly requests that the Examiner indicate consideration of all documents submitted with the IDS in the next action.

To summarize the Office Action, claims 4 and 19 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite. However, the Examiner notes that these claims would be allowable if rewritten to overcome this rejection and to include all of the limitations of the base claim and any intervening claims. Further, claims 1-3, 5-7, 16-18, and 20-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishiyama (U.S. Patent Application No. 2002/0180720 A1).

For at least the following reasons, the outstanding rejections are traversed.

Claim Rejections - 35 U.S.C. § 112

As noted above, claims 4 and 19 are rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. For instance, the Examiner alleges that the applicant does not point out in the diagram the particularities of claims 4 and 19. Applicant respectfully submits that the features of claims 4 and 19 are sufficiently clear and definite and the rejection is improper.

In particular, Applicant refers the Examiner to the exemplary, non-limiting embodiment shown in Figure 7 of the present application, which illustrates all of the features of claims 4 and 19. Applicant therefore submits that the features of claims 4 and 19 are sufficiently illustrated at least by the exemplary, non-limiting embodiment shown in Figure 7, and this ground of rejection is without merit. Reconsideration and withdrawal of the rejection is requested.

Claim Rejections - 35 U.S.C. § 102

As noted above, claims 1-3, 5-7, 16-18, and 20-21 stand rejected under 35 U.S.C. § 102 as allegedly being anticipated by Ishiyama. Applicant respectfully traverses and submits that Ishiyama fails to anticipate all the features of these claims, as evidenced by the following.

Claim 1 defines a common drive circuit for a display comprising, *inter alia*, a first voltage supply and a second voltage supply which respectively supply a high level voltage signal and a low level voltage signal to a common electrode, at least one first transistor including either a drain or a source terminal connected to the first voltage supply, at least one second transistor

including either a drain or source terminal connected to the second voltage supply, at least one signal line connected to each gate terminal of the first and second transistor, and at least one capacitance load connected to respective terminals of the first and said second transistors not connected to the first and second voltage supplies. Claim 1 further recites the features of a high level of a signal passing through the at least one signal line is the same or higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is the same or lower than the low level voltage signal supplied by the second voltage supply.

Conversely, Ishiyama discloses a ***data line*** driving circuit of a display, and fails to teach or suggest a ***common drive*** circuit for a display, as defined by claim 1. In this regard, Applicant notes that Ishiyma teaches that operational amplifiers for driving the data line are changed over corresponding to the changeover of the voltage level of the counter electrode. *See* Ishiyama at paragraphs 162-164. The data line driving circuit 20, as shown in FIG. 11A of Ishiyama, includes operational amplifiers OP1 and OP2. *See* Ishiyama at paragraphs 165-168. In operation, the pole of the voltage of the data lines Q1 and Q2 are forced to be the same pole of the voltage on data line S when the pole of the voltage on data line S is reversed. Operational amplifiers OP1 and OP2 return the pole of the voltage of data lines Q1 and Q2 to the original pole.

Thus, when the voltage of data line S transitions from high to low, since the data lines Q1 and Q2 are forced to be the same pole of the counter electrode, the operational amplifier OP1,

which has a high ability to charge, is driven. On the other hand, when the voltage of the data line S transitions from low to high, since the data lines Q1 and Q2 are forced to be the same pole of the voltage of the common electrode, the operational amplifier OP2, which has a high ability to discharge, is driven. *See* Ishiyama at paragraph 169.

However, in the data line driving circuit of Ishiyama, it is necessary for the data line driving circuit 20 to open (refer to high impedance state "HIZ", as indicated in FIG. 11B) the data line driving circuit output in order to allow the voltage of the data lines Q1 and Q2 to follow when the pole of the voltage of the counter electrode VCOM is reversed. Thus, according to Ishiyama, it is not possible to replace signal SEL1 and SEL2 with a signal and another signal, in which to poles are reversed with respect to each other because the transfer gates TG1 and TG2, or switching elements, must be "OFF" at the "HIZ" state.

Ishiyama therefore does not teach or suggest at least the features of the first voltage supply, the second voltage supply, and the at least one signal line of the claimed common drive circuit, in which a high level of a signal passing through the at least one signal line is the same or higher than the high level voltage signal supplied by the first voltage supply and a low level of the signal passing through the signal line is the same or lower than the low level voltage signal supplied by the second voltage supply. At least for the reasons noted above, the data line drive circuit of Ishiyama fails to suggest all the features of the claimed common line drive circuit for a display.

Accordingly, reconsideration and withdrawal of the rejection of claim 1 is requested. With respect to dependent claims 2-7 and 27, Applicant submits that these claims are allowable at least by virtue of depending from claim 1 and by virtue of the features recited therein.

Claim 16 defines a display comprising a substrate, a display portion integrated on the substrate, a gate driver circuit which controls switching of pixels of each line in a display portion; and a common drive circuit for said display portion which simultaneously driving capacitance loads in said display portion. Further, claim 16 recites the feature of the common drive circuit is disposed on a position opposite to said gate driver circuit and said display portion therebetween.

As discussed above, Ishiyama does not disclose a common drive circuit. Further, the data driver circuit of Ishiyama fails to suggest the arrangement of the claimed common drive circuit, which is disposed on a position opposite to said gate driver circuit and said display portion therebetween, at least for the reasons set forth in the foregoing. Accordingly, reconsideration and withdrawal of the rejection of claim 16 is requested.

With respect to claims 17-21 and 28, Applicant submits that these claims are allowable at least by virtue of their dependency and by virtue of the features recited therein. Allowance of these claims is therefore requested.

New Claims

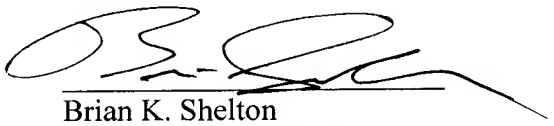
In order to provide additional coverage merited by the scope of the invention, Applicant is adding new claims 27 and 28. Applicant submits that claims 27 and 28 are allowable at least by virtue of their dependency and by virtue of the features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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